



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,817	01/26/2004	Jerome S. Culik	857 017 NP	6885
25191	7590	09/12/2005	EXAMINER	
BURR & BROWN PO BOX 7068 SYRACUSE, NY 13261-7068			DUONG, KHANH B	
			ART UNIT	PAPER NUMBER
			2822	
DATE MAILED: 09/12/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

<b>Office Action Summary</b>	<b>Application No.</b> 10/764,817	<b>Applicant(s)</b> CULIK ET AL.	
	<b>Examiner</b> Khanh B. Duong	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 July 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,48-54,57,60,62-67,69-72,75 and 76 is/are pending in the application.
- 4a) Of the above claim(s) 1 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 48-54,57,60,62-67,69-72,75 and 76 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Response to Amendment***

This office action is in response to the amendment filed on July 7, 2005.

Accordingly, claim 76 was amended.

Claim 1 remains withdrawn from further consideration as being drawn to a nonelected invention.

Claims 48-54, 57, 60, 62-67, 69-72, 75 and 76 remain active in this application.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

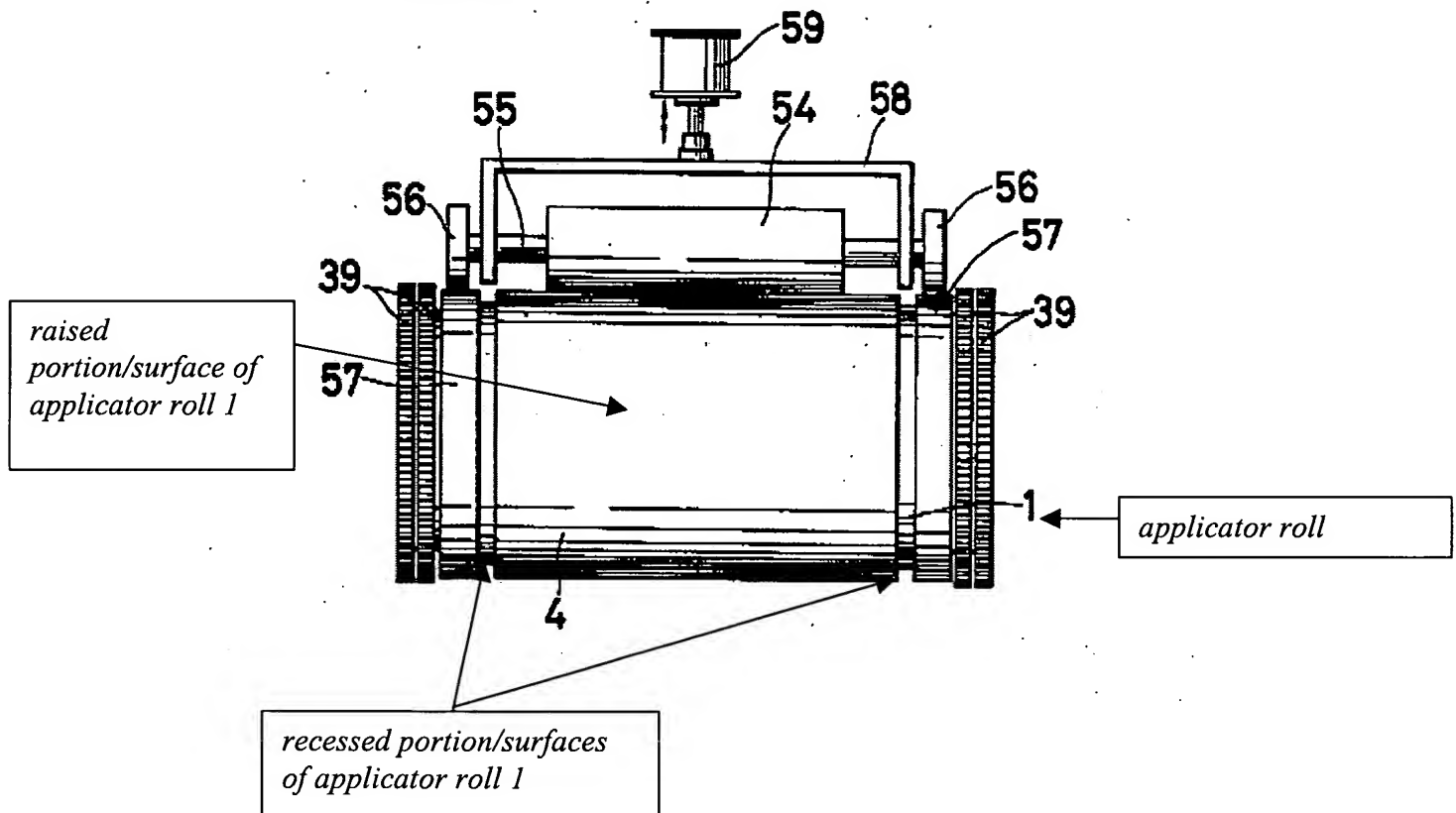
This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

Art Unit: 2822

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 71, 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki et al. (U.S. Patent No. 4,479,432) in view of Rouberol (U.S. Patent No. 6,379,569).**

Masaki et al. ("Masaki") discloses in FIG. 1 a method for applying at least one electrical contact to a semiconductor substrate, comprising: passing a semiconductor substrate 9 through a first printing space; and rotating about a first axis a first applicator roll 1 having a first roll printing surface 4 which comprises at least one raised first pattern surface [see FIG. 14], such that each said raised first pattern surface passes through a first ink space (intaglio plates 6) containing a first conductive ink 8 [see col. 9, lines 24 and 25], and through said first printing space, whereby said first conductive ink 8 is passed from at least one said raised first pattern surface onto a first semiconductor substrate surface of said semiconductor substrate 9 to deposit a first conductive ink pattern 5 on said first semiconductor substrate surface [see illustration below of FIG. 14].

**FIG. 14**

Re claim 71, Masaki fails to disclose the use of a hot melt ink.

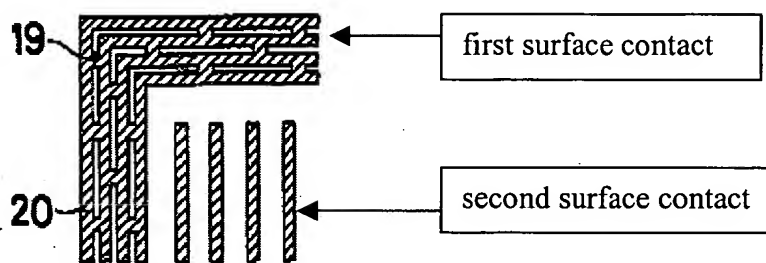
Rouberol suggests using a hot melt ink to form a mask layer [see col. 2, lines 6-57].

Since Masaki and Rouberol are from the same field of endeavor, the purpose disclosed by Rouberol would have been recognized in the pertinent prior art of Masaki.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Masaki as suggested by Rouberol, since Rouberol states at column 2, lines 45-50 that the hot melt inks have a low melting temperature and solidify on the substrate at an extremely rapid rate.

Art Unit: 2822

Re claim 75, Masaki expressly discloses in FIG. 3(b) providing a second surface contact on a second semiconductor substrate surface of said semiconductor substrate [see illustration below of FIG. 3(b)].

**FIG. 3(b)**

Re claim 76, Masaki discloses firing semiconductor substrate after printing a wiring pattern for hardening [see col. 5, lines 62-65]

**Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki and Rouberol as applied to claim 71 above, and further in view of Barajas (U.S. Patent No. 4,531,986).**

Re claim 72, Masaki and Rouberol fail to disclose using hexadecanol (cetyl alcohol).

Barajas suggests using cetyl alcohol as a solvent [see col. 4, lines 19-24].

Since Masaki, Rouberol and Barajas are from the same field of endeavor, the purpose disclosed by Barajas would have been recognized in the pertinent prior art of Masaki and Rouberol.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method disclosed by Masaki and Rouberol as

Art Unit: 2822

suggested by Barajas, since Barajas states at column 4, lines 21-24 that cetyl alcohol is desired as a solvent because it is a solid at normal temperatures, also melts, but does not evaporate, and intermixes as a liquid with the other liquid components of the vehicle.

**Claims 48-54, 57, 60, 62 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isen et al. (U.S. Patent No. 5,656,081) in view of Masaki.**

Isen et al. ("Isen") discloses in FIG. 5 a method for applying at least one electrical contact to a semiconductor substrate, comprising: passing a semiconductor substrate 6 [see FIG. 1] through a first printing space (printing station 2); rotating about a first axis a first applicator roll 64 having a first roll printing surface which comprises at least one raised first pattern surface 16 [see FIG. 4], such that each said raised first pattern surface 16 passes through a first ink space 66 containing a first conductive ink and through said first printing space; conveying said semiconductor substrate 6 from said first printing space to a second printing space (printing station 3); passing said semiconductor substrate 6 through said second printing space; and rotating about a second axis a second applicator roll 72 having a second roll printing surface which comprises at least one raised second pattern surface 16 [see FIG. 4], such that each said raised second pattern surface passes through a second ink space 74 containing a second conductive ink and through said second printing space.

Re claim 48, Isen fails to disclose using said raised first and second pattern surfaces to pass said first and second conductive inks onto said first semiconductor substrate surface of said semiconductor substrate to deposit a first conductive ink pattern on said first semiconductor substrate surface.

Masaki suggests in FIGs. 1 and 14 the use of a raised pattern 4 on an applicator roll 1 to pass conductive ink patterns 5 onto a semiconductor wafer 9 [see illustration above of FIG. 14].

Since Isen and Masaki are from the same field of endeavor, the purpose disclosed by Masaki would have been recognized in the pertinent prior art of Isen.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Isen as suggested by Masaki, since Masaki states that the transferring layer (raised pattern) 4 on the transfer cylinder improves separability for facilitating complete transfer of ink from the transferring layer onto the material to be printed [see Masaki's Abstract, lines 1-4].

Re claim 49, Isen discloses in FIG. 8 at least one region of said first conductive ink pattern 808 and at least one region of said second conductive ink pattern 810 overlap by less than 1 cm (approx. 0 cm).

Re claims 50 and 51, Isen appears to disclose in FIG. 6 said first conductive ink pattern and said second conductive ink pattern together cover substantially an entirety of said first semiconductor substrate surface, except for a border region around an edge of said first semiconductor substrate surface.

Re claims 53 and 54, Isen expressly discloses in FIG. 5 rotating a first feed roll 68 about a third axis, said first printing space (printing station 2) being defined between said first applicator roll 64 and said first feed roll 68; rotating a second feed roll 76 about a fourth axis, said second printing space (printing station 3) being defined between said second applicator roll 72 and said second feed roll 76; and drying (dryer 70) said semiconductor substrate after said



Art Unit: 2822

passing said semiconductor substrate through said first printing space and before said passing said semiconductor substrate through said second printing space.

Re claims 57 and 60, Isen expressly discloses in FIG. 8 providing a second surface contact 804 on a second semiconductor substrate surface of said semiconductor substrate 53.

Re claims 62 and 65, Isen discloses the following parameters for the conductive ink: solvent (55-85 % wt., or 25-65 % wt. if water is used), metal comprising aluminum (3-80 % wt.), binder (1-7 % wt.), and may contain silver [see col. 6, lines 13-67].

**Claims 63 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isen and Masaki as applied to claims 48-54, 57, 60, 62 and 65 above, and further in view of Rouberol.**

Re claims 63 and 66, Isen and Masaki fail to disclose the use of a hot melt ink.

Rouberol suggests using a hot melt ink to form a mask layer [see col. 2, lines 6-57].

Since Isen, Masaki and Rouberol are from the same field of endeavor, the purpose disclosed by Rouberol would have been recognized in the pertinent prior art of Isen and Masaki.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method disclosed by Isen and Masaki as suggested by Rouberol, since Rouberol states at column 2, lines 45-50 that the hot melt inks have a low melting temperature and solidify on the substrate at an extremely rapid rate.

Art Unit: 2822

**Claims 64 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isen, Masaki and Rouberol as applied to claims 48-54, 57, 60, 62, 63, 65 and 66 above, and further in view of Barajas.**

Re claims 64 and 67, Isen, Masaki and Rouberol fail to disclose using hexadecanol (cetyl alcohol).

Barajas suggests using cetyl alcohol as a solvent [see col. 4, lines 19-24].

Since Isen, Masaki, Rouberol and Barajas are from the same field of endeavor, the purpose disclosed by Barajas would have been recognized in the pertinent prior art of Isen, Masaki and Rouberol.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method disclosed by Isen, Masaki and Rouberol as suggested by Barajas, since Barajas states at column 4, lines 21-24 that cetyl alcohol is desired as a solvent because it is a solid at normal temperatures, also melts, but does not evaporate, and intermixes as a liquid with the other liquid components of the vehicle.

**Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isen and Masaki as applied to claims 48-54, 57, 60, 62 and 65 above, and further in view of Degani et al. (U.S. Patent No. 6,433,411).**

Re claims 69 and 70, Isen and Masaki fail to disclose utilizing single crystal silicon or polycrystalline silicon to form the substrate.

Degani et al. ("Degani") teaches circuit runners are printed on the top side of a substrate, wherein the substrate comprises single crystal silicon, polycrystalline silicon or amorphous silicon [see col. 7, lines 10-15 and 29-32].

Since Isen, Masaki and Degani are from the same field of endeavor, the purpose disclosed by Degani would have been recognized in the pertinent prior art of Isen and Masaki.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method disclosed by Isen and Masaki as suggested by Degani, since Degani states at column 3, lines 61-65 that such silicon substrate is “convenient to use standard IC interconnect technology, which comprises a grown or deposited oxide, and aluminum metallization interconnect patterns photolithographically formed on the oxide”.

#### ***Response to Arguments***

Applicant's arguments filed July 7, 2005 have been fully considered but they are not persuasive.

Applicant persistently argues that Masaki fails to disclose the use of a “raised pattern surface” on an applicator roll. In response, the Examiner respectfully disagrees because, as illustrated in FIG. 14 of Masaki above, the applicator roller 1 comprises a raised portion/surface relative to two recessed portions/surfaces of the roller 1. Thus, because of its raised nature, this raised portion/surface can be considered as a “raised pattern surface”.

Furthermore, it is respectfully noted the applicator roller 1 of Masaki appears to be substantially the same as the applicator roller 50 of Applicant as shown in FIG. 5.

#### ***Conclusion***

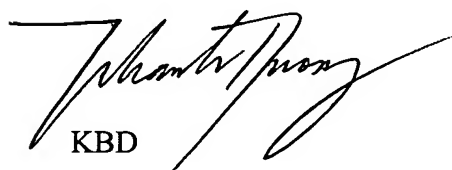
**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

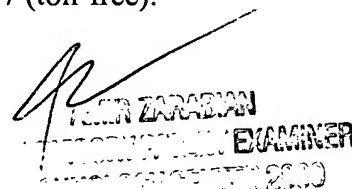
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KBD



AMIR ZARABIAN  
SUPERVISOR  
EXAMINER  
ART UNIT 2822